

PTO/8B/08A (08-03)

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**INFORMATION DISCLOSURE
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Sheet

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of

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Complete if Known

Application Number	09/595,776
Filing Date	06/16/2000
First Named Inventor	Enric Musoll
Art Unit	2183
Examiner Name	David J. Huisman
Attorney Docket Number	P3810

Examiner Initials*	Cite No. ¹	U. S. PATENT DOCUMENTS			
		Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
03H		US- 5600837 A *	02-04-1997	Arteri, Alain	
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Examiner Initials*	Cite No. ¹	FOREIGN PATENT DOCUMENTS			
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Examiner Signature	<i>David J. Huisman</i>	Date Considered	3-17-04
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Sheet 2 of 5

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U. S. PATENT DOCUMENTS					
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		Number-Kind Code ² (if known)			
		US- 6415802 *	03-18-2003	Katafatis et al.	
		US- 5535365 *	04-29-1998	Hughes et al.	
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Signature

David J. Huisman

Date
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
DJH		* FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp 210 -221, IEEE	
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DJH		* STEERE et al., "A Feedback - Driven Proportion Allocator for Real-Rate Scheduling", Third Symposium on Operating Systems Design and Implementation, February 1999, pp 145-158, USENIX Association	
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Examiner Signature	<i>David J. Huisman</i>	Date Considered	3-17-04
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Art Unit	2183
Examiner Name	David J. Huisman
Attorney Docket Number	P3810

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		* The PowerPC Architecture: A Specification for a New Family of RISC Processors, Second Edition, May 1994, pp 70-72, Morgan-Kaufmann, San Francisco	
		* MC68020 32-Bit Microprocessor User's Manual, Third Edition, 1989, pp 3-125, 3-126, and 3-127, Prentice Hall, New Jersey	
		* POTEI, M.J., Real-Time Playback in Animation Systems, Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques, 1977, pp. 72-77, San Jose, CA	
		* ARM Architecture Reference Manual, 1996, pp. 3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall	
		* ESA/390 Principles of Operation, IBM Library Server, 1993, Table of Contents and Para. 7.5.31 and 7.5.70 (available at: http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ9AR004/CONTENTS)	
		* MC88110 Second Generation RISC Microprocessor User's Manual, 1991, pp-10-66, 10-67 and 10-71, Motorola, Inc.	
		* DIFENDORFF, KEITH et al., Organization of the Motorola 88110 Superscalar RISC Microprocessor, IEEE Micro, April 1992, pp 40-63, Vol. 12, No. 2	
		* KANE, GERRY, PA-RISC 2.0 Architecture, 1996, pp 7-106 and 7-107, Prentice Hall, New Jersey	
		* DIFENDORFF, KEITH et al., Altivec Extension to PowerPC Accelerates Media Processing, March - April 2000, pp. 85-95, IEEE Micro, Vol. 20, No. 2	
DJH		* YAMAMOTO ET AL., Performance Estimation of Multistreamed, Superscalar Processors, IEEE, 1994, pp 195-204, Hawaii, US	

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		* GRUNEWALD, WINFRIED et al., Towards Extremely Fast Context Switching in a Block-Multithreaded Processor, Proceedings of EURO-MICRO-22, 1996, pp. 592-599	
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